

91/

METHOD AND APPARATUS FOR IMPROVED PERFORMANCE OF FLASH
MEMORY CELL DEVICES

Yuesong He

5

Kent Kuohua Chang

R. Lee Tan

ABSTRACT

Dopant of an n-type is deposited in the channel
10 area of a p-type well of isolated gate floating gate
NMOS transistors forming the memory cells of a memory
device array connected in a NAND gate architecture.
The dopant is provided by a tilt angle around the
existing floating gate/control gate structure at the
15 stage of the fabrication process where the floating
gate/control structure is in existence, the field
oxidation step may also have occurred, and implantation
of the source and drain dopants may also have occurred.
This forms a retrograde n-type distribution away from
20 the direction of the surface of the substrate in the
channel, which is also concentrated laterally toward
the centerline axis of the gate structure and decreases
towards the opposing source and drain regions. This
deposition promotes buried-channel-like performance of
25 the NMOS transistors connected in series in the NAND
gate memory architecture. This reduces series
resistance of the series-connected floating gate MOS
devices, allowing the desired reduction in source/drain
dopant levels in order to combat short channel effects.

30